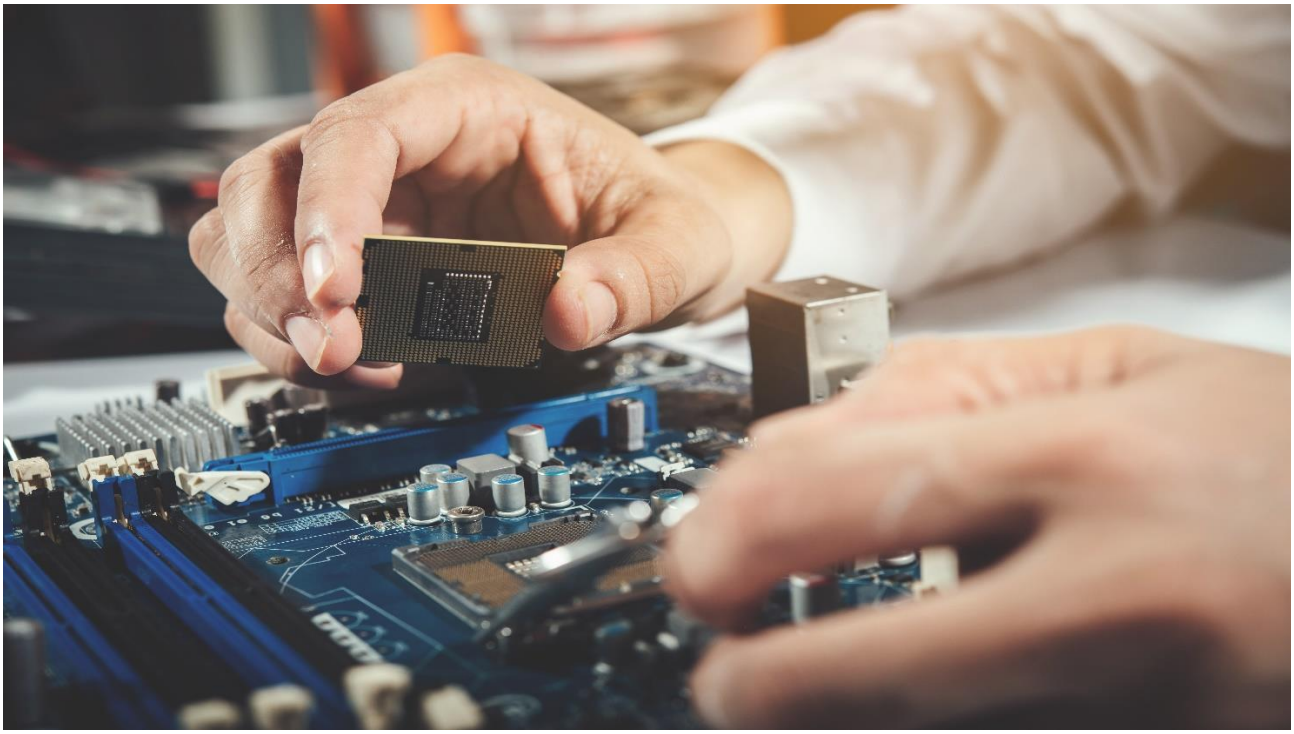

Model Curriculum

NOS Name: VLSI Design Fundamentals

NOS Code: ELE/N1419

NOS Version: 1.0

NSQF Level: 4

Model Curriculum Version: 1.0

Electronics Sector Skills Council of India || 155, 2nd Floor ESC House, Okhla Industrial Area – Phase 3, New Delhi - 110020

Table of Contents

Training Parameters

Sector	Electronics
Sub-Sector	Semiconductor & Components
Occupation	Product Design-S&C
Country	India
NSQF Level	4
Aligned to NCO/ISCO/ISIC Code	NCO-2015/2512.0501
Minimum Educational Qualification and Experience	1. 2nd year of 3 year diploma after 10th No experience required 2. 12th or equivalent No experience required 3. 10th 3 year experience required 4. Previous NSQF qualification of level 3 3 year experience required
Pre-Requisite License or Training	NA
Minimum Job Entry Age	18
Last Reviewed On	27.08.2024
Next Review Date	27.08.2027
NSQC Approval Date	27.08.2024
NOS Version	1.0
Model Curriculum Creation Date	27.08.2024
Model Curriculum Valid Up to Date	27.08.2024
Model Curriculum Version	1.0
Maximum Duration of the Course	60

Program Overview

This section summarizes the end objectives of the program along with its duration.

Training Outcomes:
At the end of the program, the learner should have acquired the listed knowledge and skills:

Compulsory:

- Basic lecture introduces different aspects of Electronics and exposure to the current activities at a particular.

Compulsory Modules:
The table lists the modules and their duration corresponding to the Compulsory NOS of the QF.

NOS and Module Details	Theory / Demonstration Duration (In Hours)	Practical/OJT Duration (In Hours)	On-the-Job Training Duration (in hours) (Mandatory)	On-the-Job Training Duration (in hours) (Recommended)	Total Duration (In Hours)
ELE/N1419	30:00	30:00	00:00	00:00	60:00
Module 1: Transistor Fundamentals and CMOS Basics	05:00	05:00	00:00	00:00	10:00
Module 2: Advanced Circuit Design Techniques	05:00	05:00	00:00	00:00	10:00
Module 3: Transistor-Level Analysis and Optimization	05:00	05:00	00:00	00:00	10:00
Module 4: Circuit Performance and Optimization	05:00	05:00	00:00	00:00	10:00
Module 5: Advanced Design Topics	05:00	05:00	00:00	00:00	10:00
Module 6: Verification, Testing, and Packaging	05:00	05:00	00:00	00:00	10:00
Total Duration	**30:00**	**30:00**	**00:00**	**00:00**	**60:00**

Module Details

Module 1: Transistor Fundamentals and CMOS Basics

Terminal Outcomes:
Upon completion of the module on Transistor Fundamentals and CMOS Basics, students will be able to:

- Demonstrate a comprehensive understanding of the fundamental properties of nMOS and pMOS transistors, including their roles in digital switching.
- Analyze and interpret the cross-sectional structure of a CMOS inverter, elucidating its fabrication steps.

Duration: 05:00 hrs
Theory - Key Learning Outcomes
• Understanding the fundamental properties of nMOS and pMOS transistors for digital switching. • Analyzing the cross-sectional structure of a CMOS inverter and its fabrication steps. • Exploring the operation of CMOS latches and flip-flops.
Duration: 05:00 hrs
Practical - Key Learning Outcomes
• Illustrating basic logic gate configurations using nMOS and pMOS transistors through schematic diagrams. • Familiarizing with stick diagrams for efficient layout planning in CMOS circuit design.
Classroom Aids: (If Offline mode)
• Whiteboard and Markers • Chart paper and sketch pens • LCD Projector and Laptop for presentations
Tools, Equipment and Other Requirements
Labs equipped with the following: • CAD tools for schematic drawing and layout planning. • Simulation software like SPICE for analyzing circuit behavior. • Visualization tools for understanding the cross-sectional structure of CMOS inverters.

Module 2: Advanced Circuit Design Techniques

Terminal Outcomes:

Upon completion of the module on Advanced Circuit Design Techniques, students will be able to:

- Generate optimized transistor-level schematics and layouts for complementary CMOS standard cells.
- Analyze the operation of D latch and D flip-flop using time diagrams.

Duration: 05:00 hrs
Theory - Key Learning Outcomes
• Proficiently generate transistor-level schematics and layouts for complementary CMOS standard cells. • Analyze the operation of D latch and D flip-flop using time diagrams, demonstrating understanding of their functionality. • Explore various techniques for managing the design of complex systems within VLSI architecture. • Understand abstraction levels of processor implementation, including architecture, microarchitecture, logic design, and physical design.
Duration: 05:00 hrs
Practical - Key Learning Outcomes
• Synthesize logic gates from hardware description language effectively. • Perform place and route operations using appropriate tools for VLSI design. • Implement optimized transistor-level schematics and layouts for CMOS standard cells. • Apply time diagrams to analyze and optimize the operation of D latch and D flip-flop circuits.
Classroom Aids: (If Offline mode)
• Whiteboard and Markers • Chart paper and sketch pens • LCD Projector and Laptop for presentations
Tools, Equipment and Other Requirements
Labs equipped with the following: • Hardware Description Language (HDL) software (e.g., Verilog or VHDL). • Electronic Design Automation (EDA) tools for place and route operations. • Simulation tools for analyzing and optimizing circuit behavior (e.g., SPICE).

Module 3: Transistor-Level Analysis and Optimization

Terminal Outcomes:

Upon completion of the module on Transistor-Level Analysis and Optimization, students will be able to:

- Investigate MOS transistor behavior across different regions using cross-sectional diagrams.
- Utilize SPICE simulation to analyze circuit performance and optimize designs effectively.

Duration: 05:00 hrs
Theory - Key Learning Outcomes
• Investigate MOS transistor behavior across different regions using cross-sectional diagrams to understand their operational characteristics thoroughly. • Derive and interpret I-V curves of MOS devices, with a focus on gate and diffusion capacitance, to analyze their electrical properties accurately. • Analyze nonideal transistor behaviors induced by high field effects and threshold voltage variations to identify and mitigate performance limitations. • Apply mathematical models to estimate MOS gate capacitance and understand its effects on circuit performance, ensuring accurate performance predictions.
Duration: 05:00 hrs
Practical - Key Learning Outcomes
• Utilize SPICE simulation tools effectively to analyze circuit performance and optimize designs based on theoretical understanding. • Conduct experiments with cross-sectional diagrams to investigate MOS transistor behavior across different regions. • Derive and interpret I-V curves of MOS devices practically, focusing on gate and diffusion capacitance, to validate theoretical knowledge. • Apply mathematical models practically to estimate MOS gate capacitance and assess its impact on circuit performance, enhancing design optimization skills.
Classroom Aids: (If Offline mode)
• Whiteboard and Markers • Chart paper and sketch pens • LCD Projector and Laptop for presentations
Tools, Equipment and Other Requirements
Labs equipped with the following: • Simulation Program with Integrated Circuit Emphasis (SPICE) software for circuit simulation and performance analysis.

Module 4: Circuit Performance and Optimization

Terminal Outcomes:

Upon completion of the module on Circuit Performance and Optimization, students will be able to:

- Explain the threshold drop in pass transistor circuits and analyze the DC response of CMOS logic gates effectively.
- Simulate circuit behavior using SPICE to analyze DC transfer characteristics, transient response, and power consumption accurately.

Duration: 05:00 hrs
Theory - Key Learning Outcomes
• Explain the threshold drop phenomenon in pass transistor circuits comprehensively to understand its impact on circuit performance. • Utilize RC delay models effectively to estimate gate delays, ensuring accurate performance predictions. • Apply Logical Effort techniques systematically to optimize combinational circuit paths and manage power consumption efficiently. • Explore the implications of technology scaling on transistor characteristics and power dissipation, considering advancements in semiconductor technology.
Duration: 05:00 hrs
Practical - Key Learning Outcomes
• Analyze the DC response of CMOS logic gates practically to understand their operational characteristics and performance limitations. • Utilize SPICE simulation tools to simulate circuit behavior accurately and analyze DC transfer characteristics practically. • Conduct experiments with RC delay models to estimate gate delays practically and validate theoretical predictions. • Apply Logical Effort techniques practically to optimize combinational circuit paths and manage power consumption effectively in real-world scenarios.
Classroom Aids: (If Offline mode)
• Whiteboard and Markers • Chart paper and sketch pens • LCD Projector and Laptop for presentations
Tools, Equipment and Other Requirements
Labs equipped with the following: • SPICE software for simulating circuit behavior and analyzing DC transfer characteristics, transient response, and power consumption.

Module 5: Advanced Design Topics

Terminal Outcomes:

Upon completion of the module on Advanced Design Topics, students will be able to:

- Architect and analyze datapath circuits effectively, including comparators, shifters, and multi-input adders.
- Understand the operations of 6T and 12T SRAM using transistor-level or gate-level diagrams accurately.

Duration: 05:00 hrs
Theory - Key Learning Outcomes
• Describe clock distribution networks comprehensively, understanding their impact on skew and power consumption. • Compare various adder architectures such as Carry-Ripple, Carry-Lookahead, and Tree Adders systematically to analyze their strengths and weaknesses. • Understand the operations of 6T and 12T SRAM using transistor-level or gate-level diagrams, ensuring a comprehensive understanding of memory design. • Explore high-speed I/O transceivers and clock recovery techniques, gaining insights into reliable data communication in integrated circuits.
Duration: 05:00 hrs
Practical - Key Learning Outcomes
• Architect and analyze datapath circuits practically, including comparators, shifters, and multi-input adders, ensuring efficient data processing in real-world applications. • Implement and optimize clock distribution networks practically to minimize skew and power consumption in integrated circuits. • Design and simulate various adder architectures such as Carry-Ripple, Carry-Lookahead, and Tree Adders practically to understand their performance characteristics. • Analyze and design high-speed I/O transceivers and clock recovery circuits practically, ensuring reliable data communication in integrated circuits.
Classroom Aids: (If Offline mode)
• Whiteboard and Markers • Chart paper and sketch pens • LCD Projector and Laptop for presentations
Tools, Equipment and Other Requirements
Labs equipped with the following: • Simulation software such as Cadence Virtuoso or Synopsys Design

Module 6: Verification, Testing, and Packaging

Terminal Outcomes:

Upon completion of the module on Verification, Testing, and Packaging, students will be able to:

- Create comprehensive test vectors for thorough testing coverage in digital circuits.
- Understand the functionality of Electrostatic Discharge (ESD) protection circuits to enhance overall chip reliability.

Duration: 05:00 hrs
Theory - Key Learning Outcomes
• Implement scan chains effectively to enhance observability and controllability during testing, facilitating efficient fault detection and debugging. • Design and integrate built-in self-test (BIST) circuits within the chip to automate the testing process and enhance reliability. • Apply IEEE standard boundary scan methodology for structural testing of integrated circuits, ensuring adherence to industry standards. • Understand the functionality of Electrostatic Discharge (ESD) protection circuits to safeguard chips against electrostatic damage effectively.
Duration: 05:00 hrs
Practical - Key Learning Outcomes
• Create comprehensive test vectors practically to detect stuck-at faults in digital circuits, ensuring thorough testing coverage. • Implement scan chains practically to enhance observability and controllability during testing, facilitating efficient fault detection and debugging. • Design and integrate built-in self-test (BIST) circuits within the chip practically to automate the testing process and enhance reliability. • Apply IEEE standard boundary scan methodology practically for structural testing of integrated circuits, ensuring adherence to industry standards.
Classroom Aids: (If Offline mode)
• Whiteboard and Markers • Chart paper and sketch pens • LCD Projector and Laptop for presentations
Tools, Equipment and Other Requirements
Labs equipped with the following: • EDA tools such as Cadence Encounter

Annexure

Trainer Requirements

Trainer Prerequisites						
Minimum Educational Qualification	**Specialization**	**Relevant Industry Experience**		**Training Experience**		**Remarks**
		Years	**Specialization**	**Years**	**Specialization**	
Graduate Science & Engineering	Electrical/ Mechanical/ Electronics	1	Semiconductor Technology, VLSI Design	1	Semiconductor Technology, VLSI Design	
Diploma/ITI	Electrical/ Mechanical/ Electronics	2	Semiconductor Technology, VLSI Design	1	Semiconductor Technology, VLSI Design	

Trainer Certification	
Domain Certification	**Platform Certification**
"**VLSI Design Fundamentals**, ELE/N1419, version 1.0". Minimum accepted score is 80%.	Recommended that the Trainer is certified for the **VLSI Design Fundamentals** "Trainer (VET and Skills)", mapped to the Qualification Pack: "MEP/Q2601, V2.0", with minimum score of 80%

Assessor Requirements

Assessor Prerequisites						
Minimum Educational Qualification	**Specialization**	**Relevant Industry Experience**		**Training Experience**		**Remarks**
		Years	**Specialization**	**Years**	**Specialization**	
Graduate Science & Engineering	Electrical/ Mechanical/ Electronics	2	Semiconductor Technology, VLSI Design	1	Semiconductor Technology, VLSI Design	
Diploma/ITI	Electrical/ Mechanical/ Electronics	3	Semiconductor Technology, VLSI Design	1	Semiconductor Technology, VLSI Design	

Assessor Certification	
Domain Certification	**Platform Certification**
"**VLSI Design Fundamentals**, ELE/N1419, version 1.0". Minimum accepted score is 80%.	Recommended that the Assessor is certified forthe **VLSI Design Fundamentals** "Assessor (VET and Skills)", mapped to the Qualification Pack: "MEP/Q2701, V2.0", with minimum score of 80%

Assessment Strategy

1. Assessment System Overview:
   - Batches assigned to the assessment agencies for conducting the assessment on SDMS/SIP or email
   - Assessment agencies send the assessment confirmation to VTP/TC looping SSC
   - Assessment agency deploys the ToA certified Assessor for executing the assessment
   - SSC monitors the assessment process & records

2. Testing Environment:
   - Confirm that the centre is available at the same address as mentioned on SDMS or SIP
   - Check the duration of the training.
   - Check the Assessment Start and End time to be as 10 a.m. and 5 p.m.
   - If the batch size is more than 30, then there should be 2 Assessors.
   - Check that the allotted time to the candidates to complete Theory & Practical Assessment is correct.
   - Check the mode of assessment—Online (TAB/Computer) or Offline (OMR/PP).
   - Confirm the number of TABs on the ground are correct to execute the Assessment smoothly.
   - Check the availability of the Lab Equipment for the particular Job Role.

3. Assessment Quality Assurance levels / Framework:
   - Question papers created by the Subject Matter Experts (SME)
   - Question papers created by the SME verified by the other subject Matter Experts
   - Questions are mapped with NOS and PC
   - Question papers are prepared considering that level 1 to 3 are for the unskilled & semi-skilled individuals, and level 4 and above are for the skilled, supervisor & higher management
   - Assessor must be ToA certified & trainer must be ToT Certified
   - Assessment agency must follow the assessment guidelines to conduct the assessment

4. Types of evidence or evidence-gathering protocol:

   - Time-stamped & geotagged reporting of the assessor from assessment location

- Centre photographs with signboards and scheme specific branding
- Biometric or manual attendance sheet (stamped by TP) of the trainees during the training period
- Time-stamped & geotagged assessment (Theory + Viva + Practical) photographs & videos

5. Method of verification or validation:

   - Surprise visit to the assessment location
   - Random audit of the batch
   - Random audit of any candidate

6. Method for assessment documentation, archiving, and access

   - Hard copies of the documents are stored
   - Soft copies of the documents & photographs of the assessment are uploaded / accessed from Cloud Storage
   - Soft copies of the documents & photographs of the assessment are stored in the Hard Drives

References

Glossary

Term	Description
Key Learning Outcome	Key learning outcome is the statement of what a learner needs to know, understand and be able to do to achieve the terminal outcomes. A set of key learning outcomes will make up the training outcomes. Training outcome is specified in terms of knowledge, understanding (theory) and skills (practical/OJT application).
Training Outcome	Training outcome is a statement of what a learner will know, understand and be able to do **upon the completion of the training**
Terminal Outcome	Terminal outcome is a statement of what a learner will know, understand and be able to do **upon the completion of a module**. A set of terminal outcomes help to achieve the training outcome.
National Occupational Standard	National Occupational Standard specify the standard of performance an individual must achieve when carrying out a function in the workplace
Persons with Disability	Persons with Disability are those who have long-term physical, mental, intellectual, or sensory impairments which in interaction with various barriers may hinder their full and effective participation in society on an equal basis with others

Acronyms and Abbreviations

Term	Description
QF	Qualification File
NSQF	National Skills Qualification Framework
NSQC	National Skills Qualification Committee
NOS	National Occupational Standards
SSC	Skill Sectors Councils
NASSCOM	National Association of Software & Service Companies
NCO	National Classification of Occupations
ISO	International Organization for Standardization
SLA	Service Level Agreement
IT	Information Technology
CRM	Customer Relationship Management
PC	Performance Criteria
PwD	Persons with Disability
SOP	Standard Operating Procedure